VC SpyGlass CDC

Smarter and faster low noise clock domain crossing verification

Overview

Among the many verification challenges confronting system-on-chip (SoC) designers today, clock domain crossings (CDC) ranks near the top in difficulty. Today's SoCs have dozens, sometimes even hundreds, of asynchronous clock domains, making it very difficult to verify using conventional simulation or static timing analysis (STA). RTL simulation is not designed to verify metastability effects, which lead to data transfer issues across asynchronous clock boundaries. STA tools also do not address asynchronous clock domain issues.

Introduction

With increasing complexity and growing chip sizes, achieving predictable design closure is a challenge, and recently CDC issues have become a leading cause of design errors. Such errors can add significant time and expense to the design-and-debug cycle and may even find their way into silicon, necessitating costly re-spins. VC SpyGlass™ provides a comprehensive methodology with scalable capacity for quality signoff with high debug productivity.

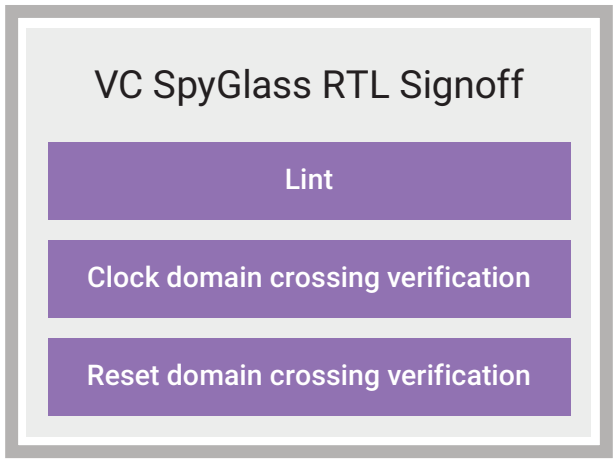

Figure 1: VC SpyGlass RTL Signoff solution

CDC Bugs

The success of static CDC verification tools is determined by two critical measures—the time taken to signoff the RTL and the completeness of CDC verification. Conventional CDC analysis tools fall short in both areas. They generate large amounts of noise (false violations), extending the verification cycle, and provide inadequate coverage on various types of CDC issues. Figure 2 describes the class of bugs/scenarios, which, if not verified correctly, can cause design re-spins. These bugs can be structural as well as functional in nature.

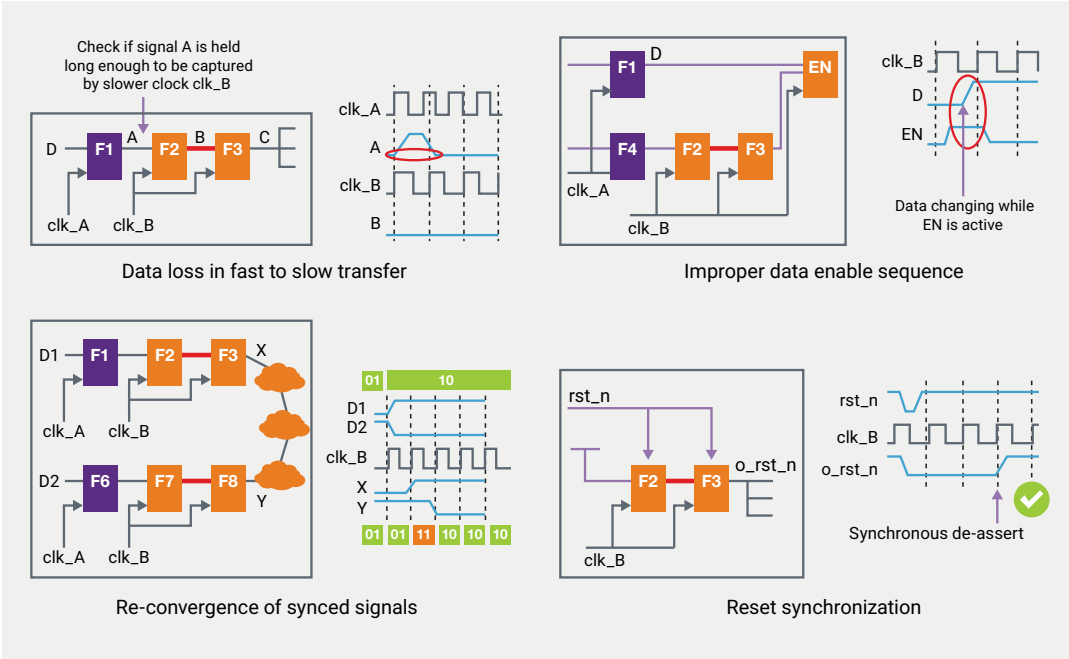

Figure 2: Typical CDC bug examples

VC SpyGlass CDC Verification

Synopsys' VC SpyGlass CDC architecture is based on six key challenges of scalable CDC verification (see Figure 3).

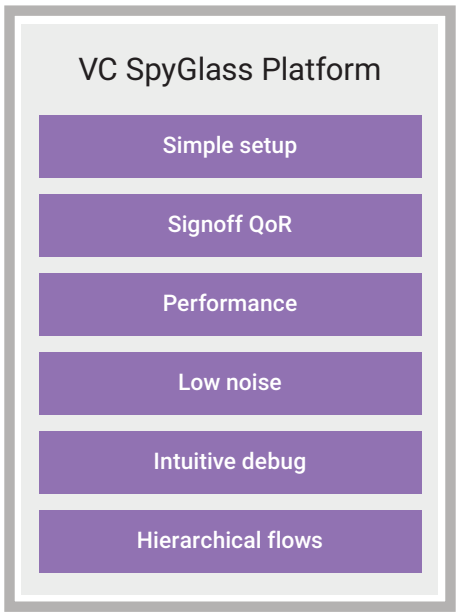

Figure 3: Scalable CDC platform addressing biggest challenges

Ease of Use and Functionality

- Utilizing existing SpyGlass SDC Constraints from current projects provides simple setup by automatically extracting the clock, reset and clock domains information
- Signoff quality using comprehensive structural and functional CDC analysis using formal and simulation based solutions
- Protocol-independent analysis, recognition of the broadest variety of synchronizers and auto-detection of quasi-static signals resulting in the lowest number of false violations
- Highest performance to achieve faster signoff and support very large designs
- Native support for UPF and SDC based CDC analysis
- Low noise with machine learning based Root Cause Analysis (RCA)
- Intuitive debug with native Verdi® integration for highest performance and CDC centric debug capabilities
- Hierarchical flows for fast turnaround using signoff abstract model
- Consistency with DesignCompiler® and PrimeTime® use models

Solving Problems at the RTL and Netlist Level

VC SpyGlass CDC provides an easy-to-use and comprehensive guide for solving CDC problems at the RTL and gate-level netlist to avoid costly re-spins.

- Methodology documentation and rule-tags integrated for direct use
- User-guided CDC methodology results in fewer, more meaningful violations, saving time for the RTL designer
- Reuse the PrimeTime® setup for netlist CDC analysis
- Guided steps for completing analysis of CDC problems at block-level as well as chip-level
  - Design setup, setup checks, design-unit integration, chip-level CDC verification, report review, and CDC verification signoff

Separating True from False Violations

Isolating real clock domain crossing issues requires detection of various synchronization schemes, not just basic two-flop or multi-flop synchronizers, and performing comprehensive protocol-independent analysis. As part of the protocol-independent analysis, VC SpyGlass CDC correlates control and data signals resulting in a good understanding of the design intent. It also detects the list of potential quasi-static signals allowing users to review the auto-generated list and use them as part of the setup. This correlation helps to produce CDC analysis with the lowest possible noise.

VC SpyGlass CDC has integrated structural and functional CDC analysis. Users make use of formal based functional CDC analysis to verify CDC protocols. Users also have the flexibility to generate System Verilog Assertions (SVA) to verify CDC protocols and assumptions made for structural analysis.

VC SpyGlass CDC also provides a signoff-quality hierarchical signoff abstract model SoC flow to perform CDC analysis for huge SoCs. This hierarchical flow helps users to use a divide-and-conquer approach to achieve the highest productivity and quickest turnaround time.

For more information about VC SpyGlass CDC and the rest of the VC SpyGlass RTL Signoff platform, visit www.synopsys.com or contact your local sales representative.